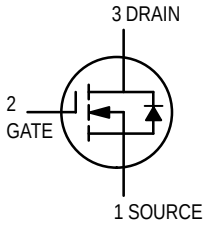
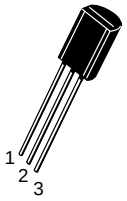
TMOS FET Transistor

N–Channel — Enhancement

VN10LM





CASE 29–05, STYLE 22
TO–92 (TO–226AE)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	60	Vdc
Gate–Source Voltage — Continuous — Non–repetitive ($t_p \leq 50$ μs)	 V_{GS} V_{GSM}	 ±20 ±40	 Vdc Vpk
Drain Current – Continuous(1) – Pulsed(2)	I_D I_{DM}	0.3 1.0	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–40 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 100 μA)	$V_{(BR)DSS}$	60	—	—	Vdc
Zero–Gate–Voltage Drain Current (V_{DS} = 45 V, V_{GS} = 0)	I_{DSS}	—	0.1	10	μAdc
Gate–Body Leakage Current (V_{GS} = –15 V, V_{DS} = 0)	$I_{GSS}1$	—	—	100	nAdc
Gate–Body Leakage Current (V_{GS} = 15 V, V_{DS} = 0)	$I_{GSS}2$	—	—	–100	nAdc

1. The Power Dissipation of the package may result in a lower continuous drain current.
2. Pulse Width ≤ 300 μs, Duty Cycle.

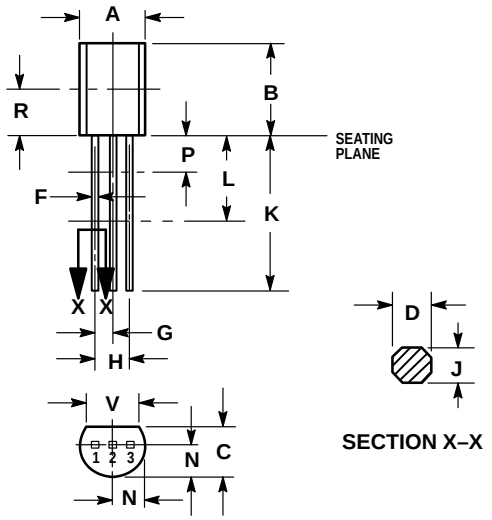
TMOS is a registered trademark of Motorola, Inc.

REV 1

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mA)	$V_{GS(th)}$	0.8	—	2.5	Vdc
On–State Drain Current (V_{DS} = 15 V, V_{GS} = 10 V)	$I_{D(on)}$	750	—	—	mA
Forward Transconductance (V_{DS} = 15 V, I_D = 500 mA)	g_{fs}	200	—	—	mmhos
Drain–Source On–Voltage (V_{GS} = 5.0 V, I_D = 200 mA)	$V_{DS(on)}$[1]	—	—	1.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 500 mA)	$V_{DS(on)}$[2]	—	—	2.5	Vdc
Drain–Source On–Resistance (V_{GS} = 5.0 V, I_D = 200 mA)	$r_{DS(on)}$[1]	—	—	7.5	Ω
Drain–Source On–Resistance (V_{GS} = 10 V, I_D = 500 mA)	$r_{DS(on)}$[2]	—	—	5.0	Ω
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	—	60	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	—	25	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	—	5.0	pF
Turn–On Time (V_{DS} = 15 V, R_L = 23 Ω, R_G = 50 Ω, V_{in} = 20 V)	t_{on}	—	—	10	ns
Turn–Off Time (V_{DS} = 15 V, R_L = 23 Ω, R_G = 50 Ω, V_{in} = 20 V)	t_{off}	—	—	10	ns

PACKAGE DIMENSIONS



SECTION X–X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSIONS D AND J APPLY BETWEEN L AND K MIMIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.44	5.21
B	0.290	0.310	7.37	7.87
C	0.125	0.165	3.18	4.19
D	0.018	0.022	0.46	0.56
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.018	0.024	0.46	0.61
K	0.500	—	12.70	—
L	0.250	—	6.35	—
N	0.080	0.105	2.04	2.66
P	—	0.100	—	2.54
R	0.135	—	3.43	—
V	0.135	—	3.43	—

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

CASE 029–05
(TO–226AE)
ISSUE AD

How to reach us:
USA / EUROPE / Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 303–675–2140 or 1–800–441–2447

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
– US & Canada ONLY 1–800–774–1848

INTERNET: http://motorola.com/sps

JAPAN: Nippon Motorola Ltd.: SPD, Strategic Planning Office, 4–32–1,
Nishi–Gotanda, Shinagawa–ku, Tokyo 141, Japan. 81–3–5487–8488

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298